IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: GEALER	Examiner: Not yet assigned
Serial No.: Not yet assigned	Group Art Unit: Not yet assigned
Filing Date: Herewith	INTEL Docket No.: P16912
For: INTEGRATED CIRCUIT PACKAGE OVERLAY	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Applicant submits herewith patents, publications or other information of which they are aware that they believe may be material to the examination of this application, and in respect of which, there may be a duty to disclose.

The filing of this information disclosure statement shall not be construed as a representation that a thorough search has been made, an admission that the information cited is, or is considered to be, material to patentability, or that no other material information exists. Nor shall the filing of this information disclosure statement be construed as an admission against interest in any manner.

This Information Disclosure Statement is filed in accordance with 37 CFR §§1.56, 1.97 and 1.98. The items listed on the accompanying Form PTO-1449 may be deemed to be pertinent to the above-identified application and are made of record to assist the Patent and Trademark Office in its examination of this application. The Examiner is respectfully requested to fully consider the items listed on the enclosed copy of Form PTO-1449 and to independently ascertain their teaching.

No fee is believed to be due under 37 CFR §1.17(p) for this Information Disclosure Statement since it is being filed concurrently with the above-identified application.

Respectfully submitted,

December 4, 2003
Date

Nandu A. Talwalkar
Registration No. 41,339
Buckley, Maschoff & Talwalkar LLC
Five Elm Street
New Canaan, CT 06840
(203) 972-0049

Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(use as many sheets as necessary)*				***Complete if Known***	
				Application Number	Not yet assigned
				Filing Date	Herewith
				First Named Inventor	GEALER
				Group Art Unit	Not yet assigned
				Examiner Name	Not yet assigned
Sheet	1	of	1	Intel Docket Number	P16923

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	A	"Integrated Circuit Packages", Copyright(C) FUJITSU LIMITED, 2002, download from http://edevice.fujitsu.com/fj/CATALOG/AD81/81-00001/11e-9.html on 12/4/2003. 1pg.	
	B	Lii, Mirng-Ji et al: "Flip-Chip Technology on Organic Pin Grid Array Packages", Intel Technology Journal Q3, 2000. 9pgs.	
	C	Mahajan, Ravi et al: "The Evolution of Microprocessor Packaging", Intel Technology Journal Q3, 2000. 10pgs.	
	D	Intel®: "The Chip Scale Package (CSP)", 2000 Packaging Databook, pages 15-1 – 15-16.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.